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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,178	09/30/2003	Shahrokh Shahidzadeh	884.912US1	6782

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER

TANG, SON M

ART UNIT	PAPER NUMBER
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2612

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/676,178

Applicant(s)

SHAHIDZADEH ET AL.

Examiner

Son M. Tang

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 November 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-29 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application
- ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chevallier [US 5,898,634] in view of Mori et al. [US 6,891,214], and further in view of Perner [US 6,694,282].

Regarding claims 12, 17-18 and 21-22 : Chevallier discloses an integrated circuit supply voltage detection circuit (200) that uses for an electronic device (i.e. portable computer), wherein the electronic device has software that performing any operation steps of the computer, the voltage detection circuit is for detecting input voltage of the IC associated with the device, the input voltage value compares with a specified voltage from the look up table (voltage ranges) to adaptively change operation of the IC [see col. 4, lines 21-24], the detected variation input voltage value range constitute of over-voltage conditions, in reflect of the Vref of the IC is 2 volts [see col. 1, lines 11-17 and col. 5, lines 40-67], and the detected over-voltage conditions output being recorded in the memory met by a (status register latch), Chevallier does not specifically disclose that recording the value corresponding to an input operating voltage. In order to determine the voltage range, the voltage value had to be recorded for comparing in the register latch. Therefore, it would have been obvious of one having ordinary skill in the art to recognize that a value corresponding to an input is being recorded in the register latch for

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determining the voltage range. Chevallier does not specifically show that determining and storing the specified/selected number of out-of specification or voltage in the memory. Mori et al. teach a memory (8) and display (9) which uses to store and display a specified/selected number of a recorded over-current or out-of-specification conditions of an operation in the IC [see Fig. 1, 12 and 9, col. 3, lines 54-66, col. 4, lines 48-58 and col. 10 lines 30-35]. It would have been obvious of one having ordinary skill in the art at the time of the claimed invention to have a selected/specified number storing and displaying as taught by Mori et al. in combination with Chevallier's invention, so that the history recorded of over-voltage specified number in the memory can be reviewed later.

Both Chevallier and Mori et al. teach the storage is a non-volatile memory, but lack of specify that the storage is an indelible memory type, Perner teaches a semiconductor component comprises a PROM memory (unchangeable data memory includes a fuse map) to store the temperature measurement [see col. 2, lines 50-67], wherein PROM memory (program read only memory) it is a one type of indelible memory. Therefore, it would have been obvious of one having ordinary skill in the art to use PROM memory to store information as taught by Perner, so the information can be protected from damage or erased.

Regarding claims 13 and 19: the combination disclose all the limitations as described above, except that not specific about filtering the operational voltage for at least a duration of one clock period. In order to determine true over-voltage condition without noise, the detection signal should be a clean signal, therefore, it would have been obvious of one having ordinary skill in the art at the time of the claimed invention to recognize that short duration (high frequency) spikes or pulses are less harmful/hazardous to the IC than longer duration (low freq.)

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true over-voltage conditions, so that a low pass filter (LPF) can be used ahead of the detector in Chevallier's invention, if such short duration/high freq. Spikes or pulses do not adversely effect the IC.

Regarding claims 14-15: The combination disclose all the limitations as described above, they fail to specify that the recording over-voltage condition is the value corresponding operation voltage greater than specified voltage (met by reference voltage V_{ref}) by two times greater than an expected noise voltage value. Since, reference voltage (V_{ref}) is a threshold value to be detected, and there is noise in the signal would need to be considered. Thus, it would have been obvious of one having ordinary skill in the art to set any appropriate tolerance (amount) value corresponding to the input operation voltage condition (selected amount) for the signal's noise, i.e. 2 times an expected noise voltage value as claimed, to prevent false detected over-voltage condition.

Regarding claim 16: The combination had made obvious above, but not specify that the system is performing a step of verifying recordation, since the electronic device is a computer which inherently has a machine-accessible medium (software) to perform the operation steps including, download data, copy data and stores data, etc., each performing step having an icon, symbol or name to indicate that the performing is completed, thus, it is obvious of one having ordinary skill in the art to recognize that the computer has software that performing a step of store data (e.g. the value corresponding to the input supply voltage) into the memory including an indication that verifying the recordation is completed or not, so user to be aware of the recordation.

Regarding claim 20: The combination disclose all the limitations as described above, Perner further teaches that the indelible memory comprises a fuse [see col. 4, lines 39-41].

Regarding claims 23 and 28: The combination disclose all the limitations as described above, Chevallier further discloses that the electronic circuit which incorporating of IC comprises a controller 162, however, Chevallier not specifically shows that controller 162 is a microprocessor, the controller and microprocessor are perform similarly functions, they both use to calculate, determine and analyze the detection voltage. Therefore, it would have been obvious of one having ordinary skill in the art to recognize that to implement the microprocessor in the electronic device of Chevallier for many benefits, including save space.

Regarding claim 24: Chevallier and combination disclose all the limitations as described above, Chevallier further discloses the detection circuit 200 which in form of a logic module [see Fig. 5].

Regarding claim 25: The combination disclose all the limitations as described above, except for not specifically teaches a logic module that comprises an analog-to digital converter, however, Chevallier further discloses that the output signal from the detector is a digital value [col. 3, lines 45-46], thus, it is obvious of one having skill in the art to recognize that the detector used some kind of converter such as an A-to-D converter to convert analog input voltage waveform to digital output prior to store in the memory.

Regarding claim 26: The combination discloses all the limitation as described above, Mori further teaches a temperature history storage unit (710) which constitutes of a second memory to store data to be compared [see col. 3, lines 44-52]. It would have been obvious of

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one having ordinary skill in the art at the time of the claimed invention to have a second memory as suggested by Mori, so that each memory unit is utilizing different function for example, memory 8 is for display and memory 710 is for determination.

Regarding claim 27: The combination disclose all the limitations as described above, Mori further teaches a recommended operations specified condition upper limit (predetermined current flows) associated with an integrated circuit they are not specifically teach a memory to store a specified condition to be compared with an operational

Regarding claim 29: The combination disclose all the limitations as described above, Mori further discloses a basic input-output system (9) [see Fig. 1].

Regarding claims 1-11: The claimed method steps are interpreted and rejected as rejection stated above.

Response to Arguments

3. Applicant's arguments filed 10/27/06 have been fully considered but they are not persuasive.

Applicant argued: (1) Chevallier does not teach detecting an over-voltage condition on any input. (2) Examiner used ordinary skill in the art (Official Notice) on rejection of claims 23 and 29. (3) PROM memory of Perner could not be used in the combination of Chevallier and Mori. (4) Chevalier reporting on a detected voltage not error condition. (5) Method claims 7, 9 and 11 rejection.

Examiner reply: (1) Chevallier's reference shows that the detection of input voltages and determines the over/under within the ranges (e.g. Vcc less than 2.6, 3.1 or greater than 3.1 etc. see Table 2), whereby, these input voltage ranges can be considered as over-voltage conditions which pre-stored in the register latch.

(2) The claimed limitations are considered and rejected as of a prima facie case of 35 U.S.C 103 obviousness, which are common to one having ordinary skill in the art, therefore, prior art evidence of any common skill in the art would unnecessary to be present.

(3) PROM memory of Perner used in the rejection is merely shows that it is obvious that PROM memory (indelible memory) is used for storing any measurement/detection data, and Application suggested that PROM memory of Perner is not compatible with Chevalier and Mori system, is only a personal opinion.

(4) The claims only claimed, that detecting over-voltage condition, which Chevallier considers as variety of input voltage ranges. The claims never claimed detecting error condition, over-voltage condition is not necessary as same error condition.

(5) The method steps of claims 7, 9 and 11 are considered as obvious included in the apparatus claims, however, Examiner further clarifies that: in claim 7, it is obvious to measure/detect any conditions occur only within a specified time period not infinity time. in claim 9, clock speed is associated with input power that including (current, voltage and resistor etc.), therefore, it is obvious that one would recording any appropriate signal that associated with power, including clock speed as user intended.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

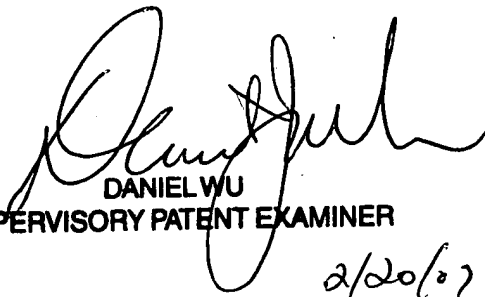
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son M. Tang whose telephone number is (571)272-2962. The examiner can normally be reached on 5/8.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Daniel J. Wu can be reached on (571)272-2964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

St


DANIEL WU
SUPERVISORY PATENT EXAMINER
2/20/07